CLAIM AMENDMENTS

Please **CANCEL** claims 10-20.

Please **AMEND** the claims as follows:

1. (Amended) A dielectric spacer structure, comprising:

a first oxide layer deposited over a top surface of a wafer and abutting a gate structure;

a silicon-nitride barrier layer deposited over said first oxide layer without having a layer of nitrided-oxide formed between said first oxide layer and said silicon-nitride barrier layer in order to reduce stress within said dielectric spacer structure caused by nitrided-oxide ~~, wherein said silicon-nitride barrier layer is formed without exposing said first oxide layer to a chemical component that nitridizes SiO_2 and Si-SiO_2 interfaces, thereby enabling formation of said silicon nitride barrier layer without nitridizing said first oxide layer~~; and

a second oxide layer formed over said silicon-nitride barrier layer.

2. (original) The dielectric spacer structure of claim 1, further comprising an etch stop nitride layer formed between said silicon-nitride barrier layer and said second oxide layer, wherein said etch stop nitride layer is formed through a process that includes ammonium precursors.

3. (original) The dielectric spacer structure of claim 1, wherein said silicon nitride barrier layer is formed through an atomic layer deposition process.

4. (amended once) The dielectric spacer structure of claim 1, wherein said silicon nitride barrier layer is formed through a~~n atomic layer~~ deposition of poly-silicon that is nitridized by a self-limiting plasma process that includes ammonia.

5. (original) The dielectric spacer structure of claim 1, wherein said silicon nitride barrier layer is formed through vapor deposition of a nitrogen-silicon gas containing a non-ammonia based organic precursor.

6. (original) The dielectric spacer structure of claim 1, wherein said silicon-nitride barrier layer is formed from vapor deposition of N_2 and $SiCl_4$.

7. (original) The dielectric spacer structure of claim 1, wherein said silicon-nitride barrier layer is formed from vapor deposition of N_2 and SiF_4.

8. (original) The dielectric spacer structure of claim 2, wherein said silicon-nitride barrier layer has a thickness of 1.5 to 3.0 nm and said etch stop nitride layer has a thickness of 30 nm to 90 nm.

9. (original) The dielectric spacer structure of claim 3, wherein said silicon-nitride barrier layer has a thickness of 30 nm to 90 nm.

10-20. (Cancelled)

Please **ADD** the following claims:

21. A method for fabricating a spacer, comprising:

forming a first SiO_2 layer over a wafer and abutting a gate structure of a MOSFET;

performing an Si_3N_4 deposition process that does not expose said first SiO_2 layer to ammonia; and

forming an Si_3N_4 layer over said first oxide layer without nitridizing said first SiO_2 layer, thereby preventing the formation of a nitrided-oxide between said SiO_2 layer and said Si_3N_4 layer.

22. A method for forming an Oxide-Nitride spacer with a reduced level of stress between the oxide and nitride layers, comprising:

forming a first SiO_2 layer abutting a gate structure of a MOSFET;

forming an Si_3N_4 layer directly on said first oxide layer; and

preventing the formation of a nitrided-oxide layer between said SiO_2 layer and said Si_3N_4 layer by depositing Nitrogen without exposing said first SiO_2 layer to ammonia, thereby reducing a level of stress at an interface between said SiO_2 layer and said Si_3N_4 layer caused by nitrided-oxide layers.

23. The method of claim 22, wherein said Si_3N_4 layer is formed by:

depositing a layer of poly-silicon directly on said SiO_2 layer; and

nitridizing said layer of poly-silicon, thereby forming said Si_3N_4 layer.

24. The method of claim 22, wherein said Si_3N_4 layer is formed by:

depositing a layer of amorphous silicon directly on said SiO_2 layer; and

nitridizing said layer of amorphous silicon, thereby forming said Si_3N_4 layer.

25. The dielectric spacer structure of claim 1, wherein said silicon nitride barrier layer is formed through an atomic layer deposition of amorphous-silicon that is nitridized by a self-limiting plasma process that includes N_2.

26. The dielectric spacer structure of claim 3, wherein said silicon nitirde barrier layer is formed through an ALD process that does not allow the formation of an oxinitride layer at an interface between said first oxide layer and said silicon nitride barrier layer.

27. The dielectric spacer structure of claim 3, wherein said silicon nitride barrier layer is formed by depositing a layer of silicon over said first oxide layer through an ALD process and subsequently nitridizing said layer of silicon.